Translation

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference T 46451WO/NZ/hs	FOR FURTHER ACTION	See Form PCT/IPEA/416
International application No. PCT/DE2004/001376	International filing date *(day/month/year)* 30.06.2004	Priority date *(day/month/year)* 03.07.2003
International Patent Classification (IPC) or national classification and IPC H01L27/00, H03K19/08, H03K19/094, H03K19/602		
Applicant POLYIC GMBH & CO. KG		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 7 sheets, including this cover sheet.

3. This report is also accompanied by ANNEXES, comprising:

   a. ☒ *(sent to the applicant and to the International Bureau)* a total of 1 sheets, as follows:

      ☒ sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).

      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.

   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s))

      _____, containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

   ☒ Box No. I Basis of the report

   ☐ Box No. II Priority

   ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

   ☐ Box No. IV Lack of unity of invention

   ☒ Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

   ☒ Box No. VI Certain documents cited

   ☐ Box No. VII Certain defects in the international application

   ☐ Box No. VIII Certain observations on the international application

CORRECTED VERSION

Date of submission of the demand	Date of completion of this report
Name and mailing address of the IPEA/EP Facsimile No.	Authorized officer Telephone No.

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
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Box No. I Basis of the report

1. With regard to the language, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

☐ This report is based on translations from the original language into the following language _____, which is the language of a translation furnished for the purposes of:

☐ international search (Rule 12.3 and 23.1(b))

☐ publication of the international application (Rule 12.4)

☐ international preliminary examination (Rule 55.2 and/or 55.3)

2. With regard to the **elements** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

☐ the international application as originally filed/furnished

☒ the description:

pages 1-7 as originally filed/furnished

pages* _____ received by this Authority on _____

pages* _____ received by this Authority on _____

☒ the claims:

nos. 2-8 as originally filed/furnished

nos.* _____ as amended (together with any statement) under Article 19

nos.* 1 received by this Authority on 18.08.2005 with letter of 16.08.2005

nos.* _____ received by this Authority on _____

☒ the drawings:

sheets 1/2-2/2 as originally filed/furnished

sheets* _____ received by this Authority on _____

sheets* _____ received by this Authority on _____

☐ a sequence listing and/or any related table(s) – see Supplemental Box Relating to Sequence Listing.

3. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages _____

☐ the claims, nos. _____

☐ the drawings, sheets/figs _____

☐ the sequence listing *(specify)*: _____

☐ any table(s) related to sequence listing *(specify)*: _____

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

☐ the description, pages _____

☐ the claims, nos. _____

☐ the drawings, sheets/figs _____

☐ the sequence listing *(specify)*: _____

☐ any table(s) related to sequence listing *(specify)*: _____

* *If item 4 applies, some or all of those sheets may be marked "superseded."*

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Box No. V **Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-8	YES
	Claims		NO
Inventive step (IS)	Claims		YES
	Claims	1-8	NO
Industrial applicability (IA)	Claims	1-8	YES
	Claims		NO

2. Citations and explanations (Rule 70.7)

1. Documents

The present report refers to the following documents:

D1: ULLMANN A ET AL: "HIGH PERFORMANCE ORGANIC FIELD-EFFECT TRANSISTORS AND INTEGRATED INVERTERS" MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS, MATERIALS RESEARCH SOCIETY, PITTSBURG, PA, US, Vol. 665, 20 April 2001 (2001-04-20), pages 265-270, XP008032774 ISSN: 0272-9172

D2: US 3 955 098 A (KAWAMOTO HIROSHI) 4 May 1976 (1976-05-04)

D3: PATENT ABSTRACTS OF JAPAN, Vol. 0030, No. 90 (E-127), 31 July 1979 (1979-07-31) &; JP 54 069392 A (NEC CORP), 4 June 1979 (1979-06-04)

2. Inventive step

Pursuant to the requirements of PCT Article 33(1), the subject matter of **claims 1-8 is not inventive** (PCT Article 33(3)).

2.1 Independent claim 1

D1 discloses (the references relate to said document):

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

An organic logic gate comprising at least one charging FET and one switching FET (figure 5), wherein the charging FET has a gate, a source and a drain electrode (figure 5).

The subject matter of **claim 1 differs from D1** in that the **gate electrode** of the charging FET is **not connected to a voltage source via a line**. In conjunction with the description (page 2, paragraph 5), the **problem of interest** can be seen as that of designing a **logic gate that switches more quickly**. D3, on the other hand, describes the problem of accelerating the switching time of the inverter gate (see PAJ abstract). The gate electrode of the charging FET is designed as a "floating" gate electrode (see PAJ abstract and figures 2 and 3). This **"floating" gate electrode** is not connected to a voltage source via a line. Although D3 describes a gate based on standard Si technology, a person skilled in the art is aware that organic and inorganic semiconductors differ from one another only on account of their materials (just as inorganic semiconductors also differ amongst each other). In the realm both of inorganic and organic semiconductors, a person skilled in the art can choose from a large number of materials. Consequently, solutions to problems from inorganic circuit technology can likewise be applied to organic circuits, and where required, the materials can be adapted to the circuit-specific requirements.

A **person skilled in the art** would therefore **apply** the teaching of **D3 to** the device of **D1** and **arrive** thereby at the subject matter of **claim 1**. He would do this without

being inventive.

In addition, attention is drawn to the fact that an **inventive step is not involved** either if **D2 or D3 is used** as the closest prior art. D2 and D3 differ from claim 1 in that they do not describe the use of organic but rather of inorganic materials. D3 shows in figures 2 and 3 an inverter with a floating gate electrode which also has a substrate connection. However, a person skilled in the art is aware that this substrate connection is only optional and does not influence the basic functionality of the inverter. The gate in D2 (figure 2A) does not have such a substrate connection.

The **problem of interest arising therefrom is that of designing a logic gate from non-inorganic material.**

However, a person skilled in the art is aware that inorganic and organic circuits differ from one another only in their materials and the associated different processing methods and electronic properties of the material. Where required, organic materials which correspond to the respective inorganic materials must be chosen. In this respect, a gate based on Si technology differs more from an As-based gate than from an organic gate since, in the latter case, a person skilled in the art has a number of materials available with which he can mimic the Si gate. The principle layout of logic gates can therefore be applied unchanged from inorganic to organic circuits.

A **person skilled in the art** would do that as a **matter of routine** and without thereby being inventive.

2.2 Dependent claims 2-8

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Claims 2-7 describe the additional features that the gate electrode of the charging FET is coupled capacitively and/or resistively to the source or drain electrode. As is apparent from figure 1 of D1, the "standard" OFET design, characterised by the overlap of the electrodes, always gives rise to a capacitive coupling between the source/drain electrodes and the gate electrode. Furthermore, the resistance between these electrodes has a finite value, and therefore it is possible also in this case to speak of a resistive coupling between the electrodes. **Claims 2-7** are therefore **not novel**.

Claim 8 discloses a logic gate that does not have a through contact. This is a trivial option which arises from the use of a floating gate, which is one of the numerous options for using the charging FET as a resistor (see also D2 and D3). A person skilled in the art would therefore choose this feature without thereby being inventive.

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Box No. VI Certain documents cited

1. Certain published documents (Rule 70.10)

Application No. Patent No.	Publication date *(day/month/year)*	Filing date *(day/month/year)*	Priority date (valid claim) *(day/month/year)*

See international search report.

2. Non-written disclosures (Rule 70.9)

Kind of non-written disclosure	Date of non-written disclosure *(day/month/year)*	Date of written disclosure referring to non-written disclosure *(day/month/year)*